International Conference on Applied Energy 2019
Aug 12-15, 2019, Västerås, Sweden
Paper ID: 423

CHARACTERISTIC ANALYSIS OF MMC-HVDC WITH FAULT AT VALVE BOTTOM OF CONVERTER

Fang Zhang [1*], Zhongyao Yang [1], Kun Chen [2], Xiaokai Chen [3], Zhengguang Chen [4], Xingguo WANG[4]

1 Key Laboratory of Smart Grid (Tianjin University), Ministry of Education, Nankai District, Tianjin 300072, China

2 Electric Power Research Institute, State Grid Hubei Electric Power Co., Ltd, Wuhan 430077, China

3 State Grid Tianjin Electric Power Company, Tianjin 300384, China

4 Grid Safety and Energy Conservation (China Electric Power Research Institute), Beijing 100084, China

ABSTRACT

Modular multilevel converter based high voltage direct current (MMC-HVDC) technology has been the preferred choice for integration of renewable energy due to its advantages in power control and transmission loss etc. This paper focused on single-line-to-ground (SLG) and three phases to ground fault at valve bottom of MMC station. Theoretical analysis of variation of AC voltage and current of MMC-HVDC, DC voltage and current, and neutral to ground current of transformer after fault occurred were conducted. Characteristics of MMC-HVDC system with fault at bottom of the valve were summarized. The theoretical analysis was verified by simulation examples. The work in this paper laid foundation for configuration of converter protection in MMC-HVDC project, thus had important engineering significance in renewable energy integration process.

Keywords: flexible DC transmission, modular multilevel converter (MMC), valve bottom fault, fault characteristic analysis

1. INTRODUCTION

Facing the increasingly severe environmental problems, renewable energy, including wind and solar power, has been widely applied in power grid. Voltage source converter based high voltage direct current (VSC-HVDC) technology has shown extensive attraction in renewable energy integration due to its inherent advantages in power control and black-start condition[1,2]. And as the most attractive topology of VSC-HVDC, modular multilevel converter (MMC), designed in module, has given its excellent performance in practice, including its high efficiency and low harmonic content [3].

Relay protection configuration is an important guarantee for steady operation of MMC-HVDC[4], which relies on fault characteristic analysis. Recently, lots of researches have been done about fault characteristic analysis. In terms of fault at AC side of MMC-HVDC, its characteristics were studied in [5], and fault ride through strategy of MMC-HVDC towards AC fault was given in [6]. Regarding DC fault, factors that can affect feature of DC fault was analyzed in [7]. As for sub-module fault, fault diagnosis and tolerant control solution was proposed in [8]. Besides, about the short-circuit fault at bridge arm, protection strategy was studied in [9].

So far, a series of researches have been carried out around the fault at AC side, DC side, sub-module and bridge arm. However, analysis aimed at fault at valve bottom of converter hasn't been fully studied. In this paper, characteristic analysis on behavior of MMC-HVDC was derived, with single-line-to-ground (SLG) and three phases to ground fault at valve bottom of converter. Then, theoretical analysis was verified through simulation in PSCAD. The results in this paper can provide theoretical basis to configuration of converter protection in MMC-HVDC project, which will benefit renewable energy integration a lot.

2. STRUCTURE OF MMC-HVDC

Fig 1 shows typical structure of MMC-HVDC system, where u_{ci} (i=1,2) is output AC voltage of MMC$_i$, P_i+jQ_i and i_{si} represent power and current flowing through PCC$_i$ respectively. R_g is grounding resistance of transformer with large value, and N$_i$ is neutral point of transformer at

Selection and peer-review under responsibility of the scientific committee of the 11th Int. Conf. on Applied Energy (ICAE2019).

MMC$_i$ side. U_{dp}, U_{dn} denote positive pole to ground voltage and negative pole to ground voltage, and U_{dci} denotes DC pole to pole voltage. i_{dp}, i_{dn} represent positive polar current and negative polar current.

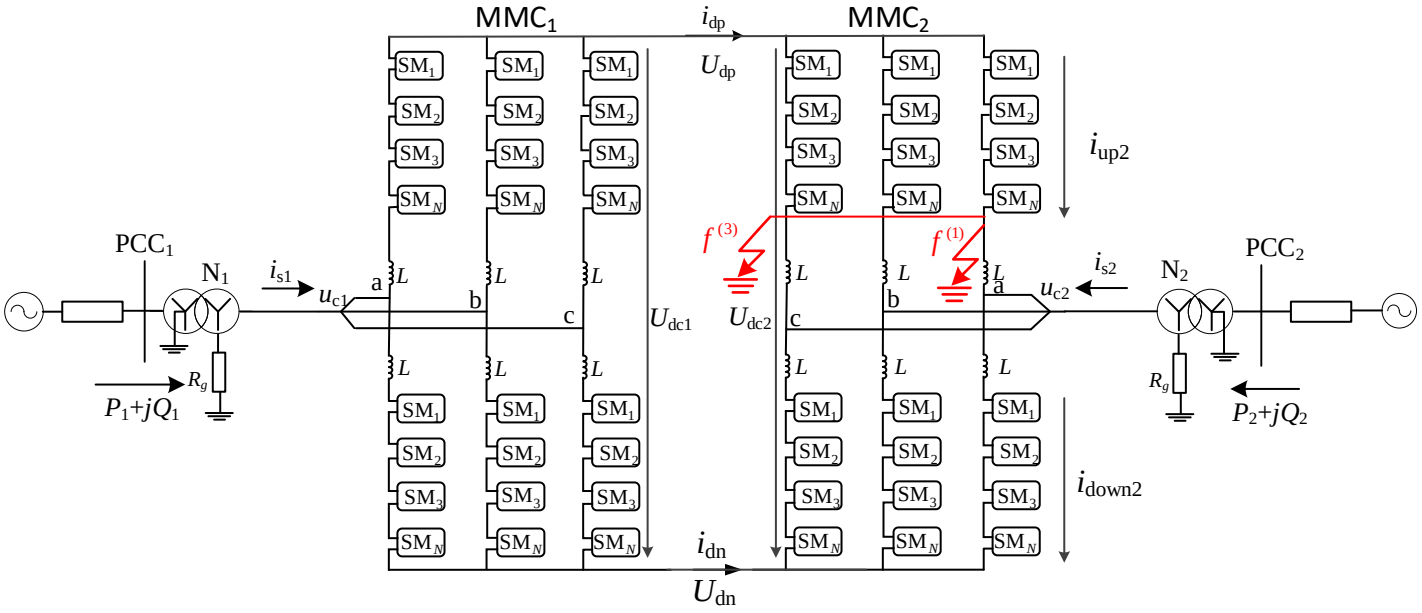


Fig 1 Diagram of MMC-HVDC system

3. CHARACTERISTIC ANALYSIS WITH SLG FAULT AT VALVE BOTTOM OF CONVERTER

In the following section, the analysis on behavior of system with SLG fault at fault point in Fig 1, will be given theoretically.

3.1 Analysis on behavior of MMC$_2$

After SLG fault occurred, phasor diagram of output AC voltage of MMC$_2$ is shown in Fig 2, where $\dot{U}_{c2\_j}(j=a,b,c)$ and $\dot{U}'_{c2\_j}(j=a,b,c)$ denote three-phase output voltage of MMC$_2$ in pre-fault condition and post-fault condition respectively, while $\dot{U}_{N2}$ and $\dot{U}'_{N2}$ denote neutral point voltage of transformer at MMC$_2$ side in pre-fault condition and post-fault condition respectively, and $\dot{U}'_{c2\_ca}$,$\dot{U}'_{c2\_bc}$,$\dot{U}'_{c2\_ab}$ denote line voltages after fault.

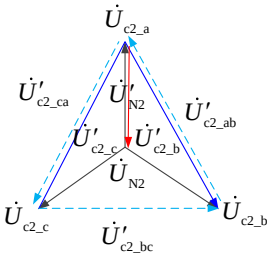


Fig 2 Phasor diagram of AC voltage of MMC$_2$

From Fig 2, it can be seen that in normal condition, N_2 is considered to be potential reference point, which implies that $\dot{U}_{N2}$ is zero, while after fault, ignoring voltage drop of arm bridge inductance, $\dot{U}'_{c2\_a}$ will drop to zero, resulting that $\dot{U}'_{N2}$ can be represented as follow: $\dot{U}'_{N2} \approx -\dot{U}_{c2\_a}$, and that $\dot{U}'_{c2\_b}$ and $\dot{U}'_{c2\_c}$ will become line voltages. By contrast, amplitudes and phases of output line voltages of MMC$_2$ will remain approximately constant after fault, resulting that i_{s2} will remain approximately same as that in normal condition. Thus, the behavior of MMC$_2$ with SLG fault at valve bottom of converter is similar with that in situation where SLG fault occurs at AC side of converter, which has been studied in [5].

When system operates at normal situation, where N_2 is considered to be potential reference point, U_{dp}, U_{dn} can be kept at $U_{dcref}/2$ and-$U_{dcref}/2$ respectively. However, after SLG fault, $\dot{U}'_{N2}$ can be represented as follow: $\dot{U}'_{N2} \approx -\dot{U}_{c2\_a}$, which has been stated above. Thus, U_{dp}, U_{dn} can be derived by (1).

$$\begin{cases} U_{dp} = U_{dcref}/2 - \dot{U}_{c2\_a} \\ U_{dn} = -U_{dcref}/2 - \dot{U}_{c2\_a} \end{cases} \quad (1)$$

Equation (1) implies that after SLG fault, U_{dp}, U_{dn} will fluctuate in sinusoidal waveform with DC bias component, resulting that after fault, U_{dc}=U_{dp}-U_{dn} can keep approximately constant compared with that in pre-fault condition.

3.2 Analysis on behavior of MMC$_1$

To analyze behavior of output AC voltage of MMC$_1$, two equations shown in (2) and (3), are derived from two perspectives of DC and AC system.

From the perspective of DC system, output AC voltage of MMC_1 can be derived by (2), when ignoring voltage drop of bridge arm inductance.

$$\begin{cases} \dot{U}'_{c1\_a} \approx \dot{U}_{ap\_a2} - \dot{U}_{ap\_a1} = \left(U_{dcref}/2 - \dot{U}_{c2\_a}\right) - \left(U_{dcref}/2 - \dot{U}_{c1\_a}\right) = \dot{U}_{c1\_a} - \dot{U}_{c2\_a} \\ \dot{U}'_{c1\_b} \approx \dot{U}_{ap\_a2} - \dot{U}_{ap\_b1} = \left(U_{dcref}/2 - \dot{U}_{c2\_a}\right) - \left(U_{dcref}/2 - \dot{U}_{c1\_b}\right) = \dot{U}_{c1\_b} - \dot{U}_{c2\_a} \\ \dot{U}'_{c1\_c} \approx \dot{U}_{ap\_a2} - \dot{U}_{ap\_c1} = \left(U_{dcref}/2 - \dot{U}_{c2\_a}\right) - \left(U_{dcref}/2 - \dot{U}_{c1\_c}\right) = \dot{U}_{c1\_c} - \dot{U}_{c2\_a} \end{cases} \quad (2)$$

where $\dot{U}_{c1\_j}(j=a,b,c)$ and $\dot{U}'_{c1\_j}(j=a,b,c)$ denote output three-phase voltage of MMC_1 in pre-fault condition and post-fault condition respectively, while $\dot{U}_{ap\_a1}, \dot{U}_{ap\_b1}, \dot{U}_{ap\_c1}$ denote arm voltage of three phases that MMC_1 generates, and $\dot{U}_{ap\_a2}$ denote arm voltage of phase a that MMC_2 generates.

And from the perspective of AC system, output AC voltage of MMC_1 can be represented by (3).

$$\begin{cases} \dot{U}'_{c1\_a} = \dot{U}_{c1\_a} + \dot{U}'_{N1} \\ \dot{U}'_{c1\_b} = \dot{U}_{c1\_b} + \dot{U}'_{N1} \\ \dot{U}'_{c1\_c} = \dot{U}_{c1\_c} + \dot{U}'_{N1} \end{cases} \quad (3)$$

Where $\dot{U}'_{N1}$ denotes neutral point voltage of transformer at MMC_1 side in post-fault condition.

By comparing equation (2) and (3), $\dot{U}'_{N1}$ can be represented as follow: $\dot{U}'_{N1} \approx -\dot{U}_{c2\_a}$. Based on analysis above, phasor diagram of output AC voltage of MMC_1 can be presented by Fig 3, where $\dot{U}'_{c1\_ca}, \dot{U}'_{c1\_bc}, \dot{U}'_{c1\_ab}$ denote output line voltages of MMC_1 after fault.

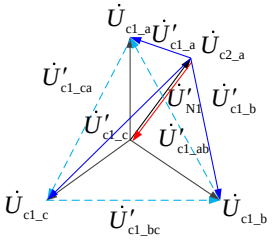


Fig 3 Phasor diagram of AC voltage of MMC_1

From Fig 3, it can be concluded that output phase voltage of MMC_1 is no longer symmetrical, while line voltages under fault condition, can remain approximately same as that in normal condition.

In normal condition, d-q components of output phase voltage of MMC_1 can be represented by (4), where P denotes Park's transformation matrix.

$$\begin{bmatrix} U_{c1\_d} \\ U_{c1\_q} \\ U_{c1\_0} \end{bmatrix} = P \begin{bmatrix} U_{c1\_a} \\ U_{c1\_b} \\ U_{c1\_c} \end{bmatrix} \quad (4)$$

As for the post-fault condition, combining (3) and (4), d-q components of output phase voltage of MMC_1 can be represented by (5).

$$\begin{bmatrix} U'_{c1\_d} \\ U'_{c1\_q} \\ U'_{c1\_0} \end{bmatrix} = \begin{bmatrix} U_{c1\_d} \\ U_{c1\_q} \\ U_{c1\_0} \end{bmatrix} + P \begin{bmatrix} \dot{U}'_{N1} \\ \dot{U}'_{N1} \\ \dot{U}'_{N1} \end{bmatrix} = \begin{bmatrix} U_{c1\_d} \\ U_{c1\_q} \\ U_{c1\_0} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \dot{U}'_{N1} \end{bmatrix} \quad (5)$$

From (5), it can be seen that d-q components of output voltage of MMC_1 can remain same as that in pre-fault condition.

Based on d-q coordinate system, the active power and reactive power injected in MMC_1, can be represented by (6)[10].

$$\begin{cases} P_1 = \frac{3}{2}\left(U_{c1d} I_{s1d} + U_{c1q} I_{s1q}\right) \\ Q_1 = -\frac{3}{2}\left(U_{c1d} I_{s1q} - U_{c1q} I_{s1d}\right) \end{cases} \quad (6)$$

Where I_{s1d} and I_{s1q} denote d-q components of the current injected in MMC_1. As MMC_1 operates at active power control and reactive power control mode, after fault, P_1 and Q_1 in (6) will remain constant with the effect of controllers in MMC_1. Meanwhile, as shown above, d-q components of output voltage of MMC_1 U'_{c1d} and U'_{c1q} can also remain same as that in pre-fault condition. Thus, I_{s1d} and I_{s1q} in (6) will remain constant after fault, and it can be derived that current injected in MMC_1 will remain same as that in normal condition, when SLG fault occurred.

As for behavior of U_{dp}, U_{dn} at MMC_1 side, it is same as that at MMC_2 side, which has been shown in section 3.1.

3.3 Analysis on behavior of DC system

In terms of U_{dc}, it will basically keep constant after fault, which has been analyzed in section 3.1.

In the following subsection, current flowing through DC line will be analyzed. As the analysis above has stated, when fault occurred, neutral point voltage of two transformers connected with MMC_1 and MMC_2 respectively will no longer equal to zero, so that short-circuit current circuit can be established through fault point and both of neutral point of two transformers as shown in Fig 4.

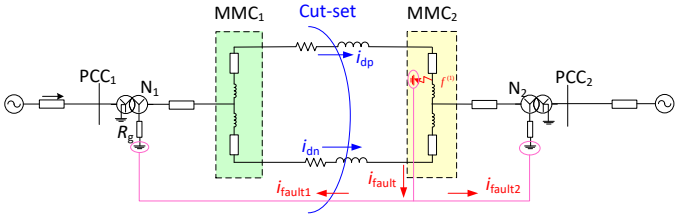


Fig 4 Diagram of short circuit current after SLG fault

Where i_{fault1} (i_{fault2}) denotes current flowing into transformer connected with MMC_1 (MMC_2) through N_1 (N_2), and i_{fault} denotes current flowing into ground through short-circuit point.

According to cut-set in Fig 4 along with Kirchhoff's current law, after fault, sum of i_{dp} and i_{dn} is not zero, but equal to i_{fault1}, which is numerically equal to ratio of $\dot{U}'_{N1}$ to R_g. Thus, the smaller R_g at MMC_1 side is, the larger deviation of sum of i_{dp} and i_{dn} from zero is, from which SLG fault at valve bottom of converter can be detected.

4. CHARACTERISTIC ANALYSIS WITH THREE PHASES TO GROUND FAULT AT VALVE BOTTOM OF CONVERTER

In the following section, the analysis on behavior of system with three phases to ground fault at fault point in Fig 1, will be given theoretically.

4.1 Analysis on behavior of MMC_2

When MMC-HVDC operates in normal condition, positive pole to ground voltage at MMC_2 side is $U_{dcref}/2$. However, in initial stage after three phases to ground fault, as voltage of fault point will drop to zero and voltages of three phases upper bridge arm are different from each other at fault instant, to keep $U_{dp\_j(j=a,b,c)}$ in same value, the sub-module capacitor in upper bridge arm will discharge quickly, which will generate short-circuit impulse current in upper bridge arm. Thus, positive pole to ground voltage at MMC_2 side will drop to zero after three phases to ground fault and remain approximately constant afterwards.

Considering that DC voltage controller of MMC_2 is set to control DC voltage at U_{dcref}, sub-module capacitor in lower bridge arm will be charged by AC system. Thus, after fault, pole to pole voltage will attempt to recover to U_{dcref}, while negative pole to ground voltage will gradually drop to $-U_{dcref}$.

As analyzed above, sub-module capacitor in lower bridge arm will be charged by AC system, thus, active power will be transmitted from AC system to MMC_2, and magnitude of current injected in MMC_2 will increase until the end of charging process of capacitor in lower bridge arm, so that magnitude of output phase voltage of MMC_2 will decrease at the beginning, and then increase with the end of charging process.

4.2 Analysis on behavior of MMC_1

As for MMC_1 side, to maintain balance of DC voltage at both MMC_1 side and MMC_2 side, in initial stage after three phases to ground fault, sub-module capacitor at MMC_1 side will discharge through DC line, upper bridge arm of MMC_2 and short circuit point, until DC voltage at MMC_1 side is equal to DC voltage at MMC_2 side, and then, sub-module capacitor at MMC_1 side will get charged. Therefore, DC voltage at MMC_1 side will gradually recover to U_{dcref}, after a period of adjustment.

Output AC voltage of MMC_1, U_{c1}, can be represented by (7), where n_{down} denotes number of conducting sub-module in lower bridge arm, and U_c denotes voltage of sub-module capacitor.

$$U_{c1} = U_{dn} + n_{down} U_c \tag{7}$$

As analyzed above, after three phases to ground fault, U_{dn} will drop from $-U_{dcref}/2$ to $-U_{dcref}$ gradually, so it can be seen from (7) that output AC voltage of MMC_1 will contain DC bias component, which is approximately $-U_{dcref}/2$. And the magnitude of the AC current injected in MMC_1 will increase until the end of charging process of sub-module capacitor at MMC_1 side.

4.3 Analysis on behavior of DC system

The pole to pole voltage of dc system will drop quickly at fault instant, and recover to U_{dcref} gradually under control of DC voltage controller at MMC_2 side, which has been analyzed in section 4.1.

To analyze DC current of MMC-HVDC, circuit of system after fault can be represented in Fig 5.

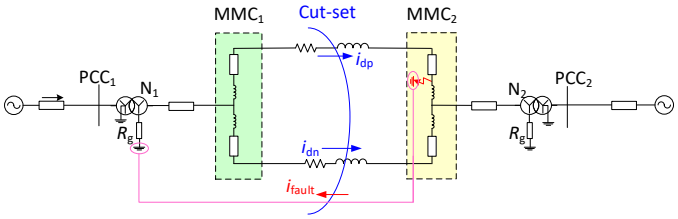


Fig 5 Diagram of short circuit current after three phases to ground fault

Where i_{fault} denotes current flowing into transformer connected with MMC_1 through N_1.

After fault, magnitude of DC current will increase, until the end of charge-discharge process of sub-module capacitor. After fault, considering cut-set in Fig 5 along with Kirchhoff's current law, sum of i_{dp} and i_{dn} is equal to i_{fault}, which is numerically equal to ratio of DC bias component of AC voltage at MMC_1 side to R_g at MMC_1 side.

5. SIMULATIONS AND VALIDATION

5.1 Case introduction

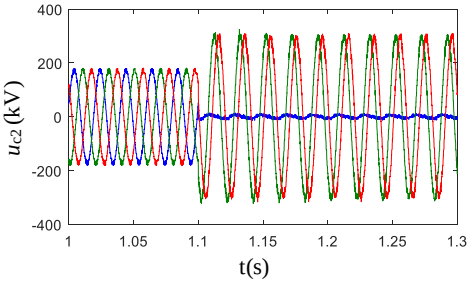
To verify theoretical analysis above, model based on Fig 1 was built in PSCAD, the main parameters of which are given in Tab 1. Note that MMC_1 operates at active power control and reactive power control mode, references of which are P_{ref}=400MW and Q_{ref1}=0MVar, while MMC_2 operates at DC voltage control and reactive power control mode, references of which are U_{dcref}=400kV and Q_{ref2}=0MVar.

Tab 1 System parameters of MMC-HVDC

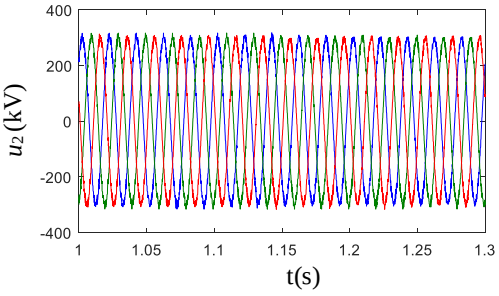
Parameters	Value
Transformer capacity	480MVA
Transformer ratio	525kV/200kV
Transformer leakage inductance	0.15p.u.
Transformer grounding resistance	1000Ω
Number of SMs per arm	20
Sub-module capacitor	3100μF
Inductance of arm inductor	40mH

5.2 Verification on analysis of behavior with SLG fault at valve bottom of converter

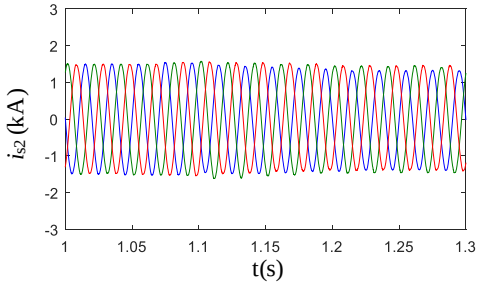
MMC-HVDC operates in normal condition originally, while SLG fault at fault point in Fig 1 occurs at 1.1s. The behavior of AC voltage and current at MMC_2 side is shown in Fig 6. As shown in Fig 6, after fault, output voltage of MMC_2 of fault phase drops to zero, while voltages of other phases become line voltages, in the meantime, output line voltage of MMC_2 and AC current injected in MMC_2 will remain approximately same as that in pre-fault condition, which is consistent with the theoretical analysis in section 3.1.



(a) Phase voltage at MMC_2 side



(b) Line voltage at MMC_2 side



(c) AC current at MMC_2 side

Fig 6 AC variables at MMC_2 side

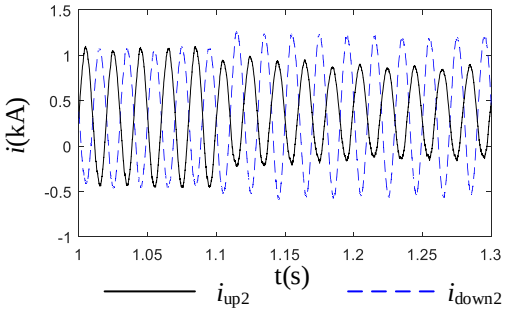
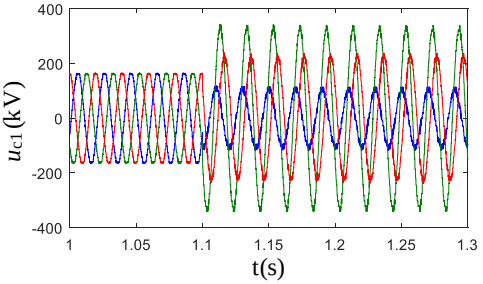
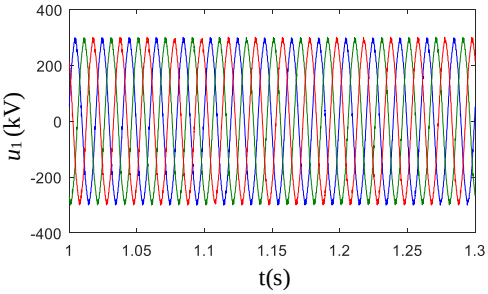


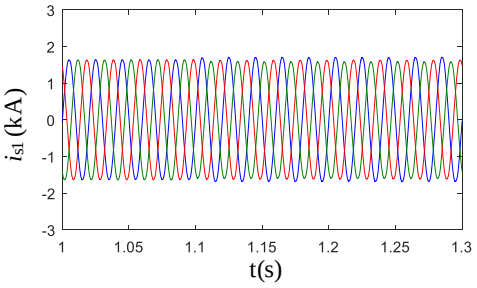
Fig 7 upper and lower bridge arm currents of MMC_2



(a) Phase voltage at MMC_1 side



(b) Line voltage at MMC_1 side



(c) AC current at MMC_1 side

Fig 8 AC variables at MMC_1 side

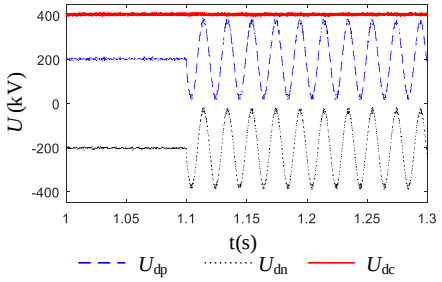


Fig 9 DC voltage of MMC-HVDC

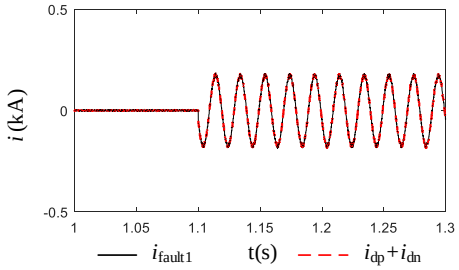


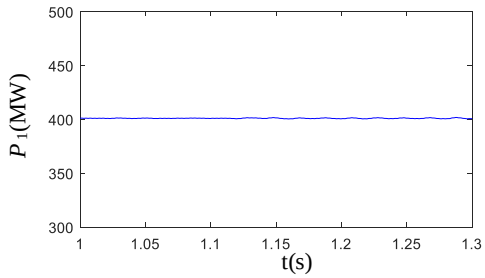
Fig 10 Comparison between i_{fault1} and $i_{dp}+i_{dn}$

The behavior of currents flowing through upper and lower bridge arm of MMC_2 is shown in Fig 7. As shown in Fig 7, after fault, lower bridge arm of MMC_2 will increase, while upper bridge arm of MMC_2 will decrease, which should be considered in configuration of converter protection in MMC-HVDC project.

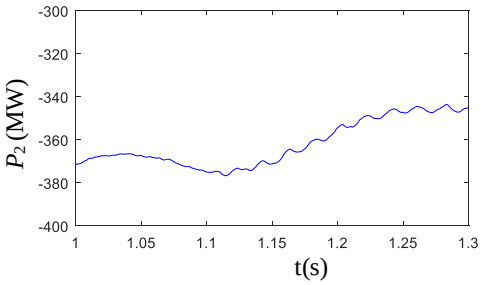
The behavior of AC voltage and current at MMC_1 side is shown in Fig 8. As shown in Fig 8, after fault, output phase voltage of MMC_1 is no longer symmetrical, while output line voltage of MMC_1 and current injected in MMC_1 under fault condition can remain approximately same as that in pre-fault condition, which is consistent with analysis in section 3.2.

The behavior of DC voltage of MMC-HVDC is shown in Fig 9, and comparison between i_{fault1} and $i_{dp}+i_{dn}$ is shown in Fig 10. As shown in Fig 9, after fault, U_{dp}, U_{dn} will fluctuate in sinusoidal waveform with DC bias component, while after fault, U_{dc} can keep approximately constant compared with that in pre-fault condition. As shown in Fig 10, after fault, sum of i_{dp} and i_{dn} is not zero, but equal to i_{fault1}. The simulation results verify the theoretical analysis in section 3.

The behaviors of active power flowing through PCC_1 and PCC_2 are shown in Fig 11. As shown in Fig 11(a), after fault, active power flowing through PCC_1 will keep constant, as MMC_1 operates at active power control and reactive power control mode. As shown in Fig 11(b), after fault, active power flowing through PCC_2 will drop to 350MW. The difference between P_1 and P_2 mainly results from power loss on resistance of DC Line, power loss on transformers and power loss caused by effect that i_{fault1} and i_{fault2} have on grounding resistance of transformer.



(a) Active power flowing through PCC_1



(b) Active power flowing through PCC_2

Fig 11 Active power flowing through PCC_1 and PCC_2

5.3 Verification on analysis of behavior under three phases to ground fault at valve bottom of converter

MMC-HVDC operates in normal condition originally, while three phases to ground fault at fault point in Fig 1 occurs at 1.1s.

The behavior of currents flowing through upper and lower bridge arm of MMC_2 is shown in Fig 12. As shown in Fig 12, the magnitude of the currents flowing through upper and lower bridge arm of MMC_2 will increase to a high value at fault instant, which should be considered in configuration of converter protection in MMC-HVDC project.

The behavior of AC voltage and current at MMC_2 side is shown in Fig 13. As shown in Fig 13, after fault, magnitude of output phase voltage of MMC_2 will decrease at the beginning, and then gradually increase, while magnitude of current injected in MMC_2 will increase at the beginning, and gradually decrease, which is consistent with the theoretical analysis in section 4.1.

The behavior of AC voltage and current at MMC_1 side is shown in Fig 14. As shown in Fig 14, after fault, output AC voltage of MMC_1 will contain DC bias component which is approximately -200kV, while magnitude of current injected in MMC_1 will increase at the beginning, and gradually decrease, which is consistent with analysis in section 4.2.

The behavior of DC voltage and current of MMC-HVDC is shown in Fig 15 and Fig 16, and the current of transformer neutral point to ground at MMC_1 side is shown in Fig 17. As shown in Fig 15, after fault, U_{dp} will drop to zero at fault instant and remain approximately constant afterwards. U_{dn} will drop from -200kV to -400kV gradually. And U_{dc} will drop quickly at fault instant and attempt to recover to 400kV gradually. As shown in Fig 16, in initial stage after fault, magnitude of i_{dp} and i_{dn} will increase firstly after fault, and gradually decrease. And comparing Fig 16 and Fig 17, sum of i_{dp} and i_{dn} is equal to i_{fault}. The simulation results verify the theoretical analysis in section 4.

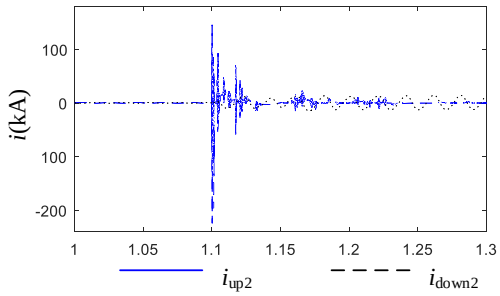
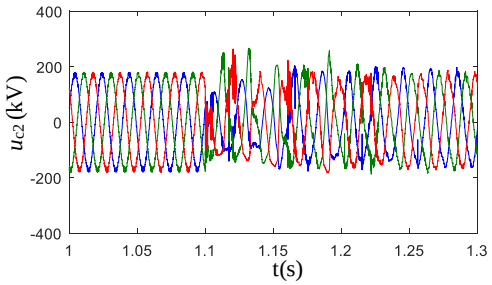
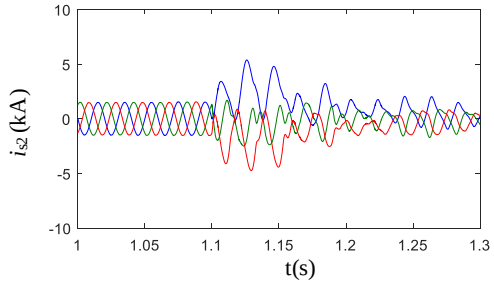


Fig 12 upper and lower bridge arm currents of MMC_2

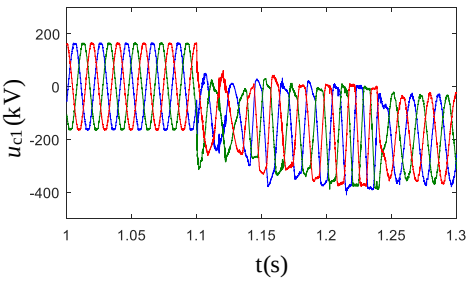


(a) Phase voltage at MMC_2 side

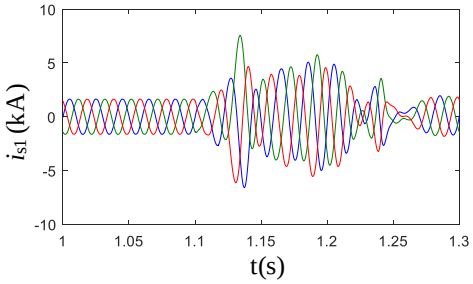


(b) AC current at MMC_2 side

Fig 13 AC variables at MMC_2 side



(a) Phase voltage at MMC_1 side



(b) AC current at MMC_1 side

Fig 14 AC variables at MMC_1 side

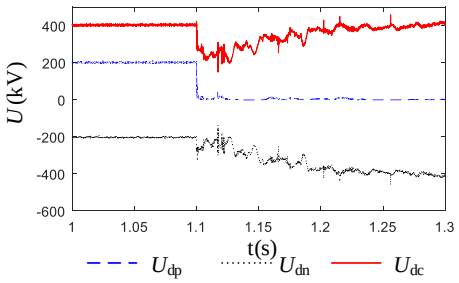


Fig 15 DC voltage of MMC-HVDC

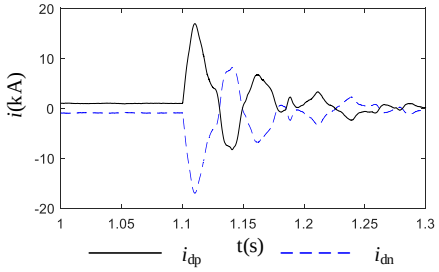


Fig 16 DC current of MMC-HVDC

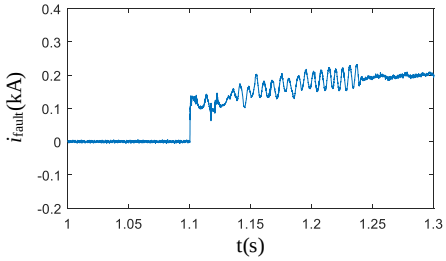


Fig 17 The current of transformer neutral point to ground at MMC_1 side

6. CONCLUSIONS

In this paper, characteristic analysis on behavior of MMC-HVDC was investigated, with different types of fault at valve bottom of converter. The conclusion summarized from theoretical analysis can be expressed as below:

Characteristics of behavior of MMC-HVDC under SLG fault can be summarized below:

(1) After fault, output voltage of MMC_2 at fault phase will drop to zero, while voltages of other phases become line voltages. Meanwhile, output line voltage of MMC_2 and AC current injected in MMC_2 will be approximately same as that in pre-fault condition.

(2) After fault, output phase voltage of MMC_1 is no longer symmetrical, while line voltages and current at MMC_1 side under fault condition can remain approximately same as that in pre-fault condition.

(3) After fault, positive pole to ground voltage and negative pole to ground voltage will fluctuate in sinusoidal waveform with DC bias component, while DC voltage can basically keep constant. And the sum of currents flowing in positive pole line and negative pole

line is not zero, but equal to transformer neutral point to ground current at MMC_1 side. The smaller neutral resistance of transformer at MMC_1 side is, the larger deviation of sum of positive pole current and negative pole current from zero is, from which SLG fault at valve bottom of converter can be detected.

(4) The active power transmitted by MMC-HVDC has a little change after SLG fault, which implies that SLG fault has a little effect on active power transmission of MMC-HVDC.

Characteristics of behavior of MMC-HVDC under three phases to ground fault can be summarized below:

(1) After fault, the magnitude of the currents flowing through upper and lower bridge arm of MMC_2 will increase to a high value at fault instant, which should be considered in configuration of converter protection in MMC-HVDC project.

(2) After fault, magnitude of output phase voltage of MMC_2 will decrease at the beginning, and gradually increase, while magnitude of current injected in MMC_2 will increase at the beginning, which implies that overcurrent phenomena will happen during the fault period.

(3) After fault, output AC voltage of MMC_1 will contain DC bias component which is approximately $-U_{dcref}/2$, while magnitude of current injected in MMC_1 will increase at the beginning, which implies that overcurrent phenomena will happen during the fault period.

(4) After fault, positive pole to ground voltage will drop to zero quickly and remain approximately constant afterwards, and negative pole to ground voltage will drop from $-U_{dcref}/2$ to $-U_{dcref}$ gradually, while DC voltage will drop quickly at fault instant and attempt to recover to the value of the normal condition gradually. And after fault, magnitude of DC current will increase firstly and gradually decrease.

The research in this paper can provide theoretical basis to configuration of converter protection in MMC-HVDC project, which will benefit renewable energy integration a lot.

ACKNOWLEDGEMENT

This work was supported by Open Fund of Power Grid Safety and Energy Conservation (No. JBB51201801311).

REFERENCE

[1] Sun J, Li M, Zhang Z, et al. Renewable energy transmission by HVDC across the continent: system challenges and opportunities. CSEE Journal of Power and Energy Systems 2017; 3(4): 353-364.

[2] Ogunrinde O, Shittu E, Dhanda K K. Investing in Renewable Energy: Reconciling Regional Policy With Renewable Energy Growth. IEEE Engineering Management Review 2018; 46(4): 103-111.

[3] Debnath S, Qin J, Bahrani B, et al. Operation, control, and applications of the modular multilevel converter: A review. IEEE transactions on power electronics 2015; 30(1): 37-53.

[4] Wang S, Li C, Adeuyi O D, et al. Coordination of MMCs with Hybrid DC Circuit Breakers for HVDC Grid Protection. IEEE Transactions on Power Delivery 2019; 34(1): 11-22.

[5] Ma S, Xu J, Wu G, et al. Characteristic investigation of MMC-HVDC system under internal AC bus fault conditions. The Journal of Engineering 2019; 2019(16): 2228-2232.

[6] Cui S, Lee H J, Jung J J, et al. A comprehensive AC-side single-line-to-ground fault ride through strategy of an MMC-based HVDC system. IEEE Journal of Emerging and Selected Topics in power Electronics 2018; 6(3): 1021-1031.

[7] Tang G, Xu Z, Zhou Y. Impacts of three MMC-HVDC configurations on AC system stability under DC line faults. IEEE Transactions on Power Systems 2014; 29(6): 3030-3040.

[8] Li B, Shi S, Wang B, et al. Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters. IEEE Transactions on Power Electronics 2016; 31(4): 3165-3176.

[9] Zhou Yang, He Zhiyuan, Pang Hui, et al. Protection of converter grounding fault on MMC based bipolar HVDC systems. Proceedings of the CSEE 2015; 35(16): 4062-4069

[10] Ferrero A, Superti-Furga G. A new approach to the definition of power components in three-phase systems under nonsinusoidal conditions. IEEE Transactions on Instrumentation & Measurement 1991; 40(3):568-577.