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Analytical Switching Loss Modeling for SiC MOSFETs Based Traction Systems for Electric Vehicles

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ABSTRACT

In this paper, the loss of silicon carbide (SiC) MOSFETs based electric vehicle (EV) traction systems are investigated comprehensively. The loss of SiC MOSFETs are analyzed and modeled based on the commutation process in the inverter. The analysis model includes parasitic inductance, parasitic capacitance nonlinearity, transconductance nonlinearity, body diode reverse recovery, and parasitic capacitance charging and discharging. The simulation results confirm the losses models of SiC MOSFETs.

Keywords: SiC MOSFETs, Electric vehicle traction systems, Losses

NONMENCLATURE

Abbreviations

EV	Electric Vehicle
SiC	Silicon Carbide
ZVS	Zero Voltage Switching

Symbols

$V_{\text{gs\_max}}$, $V_{\text{gs\_min}}$	Maximum and minimum gate drive voltage
C_{gs} C_{gd} C_{ds}	Parasitic capacitance
V_{dc} / I_0	Bus voltage/Load current
$R_{\text{g\_int}}$ / $R_{\text{g\_ext}}$	Internal /External gate resistance
L_{d} L_{s} L_{pcb}	Parasitic inductance
rr	Body diode reverse recovery

1. INTRODUCTION

Electric vehicle (EV) traction systems are undergoing significant changes with the application of wide band-gap semiconductor devices, such as silicon carbide (SiC) or gallium nitride (GaN) MOSFETs, according to their increased high switching speeds, lower on-resistance, greater thermal conductivity, and higher junction temperatures[1]. High switching speed plays an important role in reducing switching losses, reducing dead time, and improving switching frequency capabilities. However, the switching loss increases as the switching frequency increases, which will influence the size of the heat dissipation system. Therefore, accurate switching loss modeling is the key to designing the electric vehicle traction systems.

Many scholars investigate the loss of SiC MOSFETs by establishing analytical models. The simplest analysis loss model is to treat the turn-on and turn-off current and voltage waveforms of the MOSFET as piecewise linear, which did not include parasitic parameters in PCB layout and device packaging. Ref[2] and [3] proposed an accurate analysis model to calculate the switching loss of SiC,which took the nonlinearity of power device capacitance and parasitic inductance in the circuit into account. Ref [4] proposed an analysis model which included parasitic inductance, nonlinear junction capacitance,and nonlinear transconductance coefficient.The above work focuses on the losses of SiC based on the double pulse test circuit.However, the actual inverter commutation process is not considered. In addition, the channel current i_{ch} is considered the source of switching loss, this paper distinguishes the channel current and the output capacitor charge and discharge current I_{oss} .

This paper first analyzes the operating mechanism of the SiC MOSFETs half-bridge in the EV traction system, then investigates the switching process and the current path at different stages in detail, and establishes the loss analysis expressions according to the different stages of turn-on and turn-off. Finally, the simulation results confirm the loss models.

2. COMMUTATION MECHANISM OF SIC MOSFETS HALF-BRIDGE IN THE EV TRACTION SYSTEM

Fig.1 is a simplified half-bridge topology of SiC MOSFETs. A and B represent the current flowing into the

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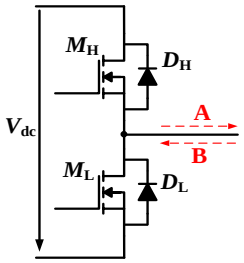
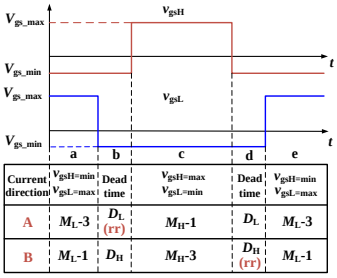


Fig.1 SiC half-bridge topology



Current direction	$V_{gsH=min}$ $V_{gsL=max}$	Dead time	$V_{gsH=max}$ $V_{gsL=min}$	Dead time	$V_{gsH=min}$ $V_{gsL=max}$
A	M_L-3	D_L (rr)	M_H-1	D_L	M_L-3
B	M_L-1	D_H	M_H-3	D_H (rr)	M_L-1

Fig.2 The conduction of half-bridge SiC with different current directions

motor (positive direction) and out of the motor (negative direction), respectively. Figure 2 shows the conduction of SiC MOSFETs half-bridges in different current directions.

As shown in Fig.2 and Fig.3, when M_H is turned off and M_L is turned on, the current flows through the third quadrant channel of M_L (Fig.3(a)); Both M_H and M_L are turned off. At this time, it is the dead time,the current commutates from the third quadrant channel of M_L to the body diode D_L(Fig.3(b)); When M_H is turned on and M_L is turned off, the current flows through the first quadrant channel of M_H (Fig.3(c)),meanwhile,the voltage across the body diode D_L changes from forward to reverse and a reverse recovery current is generated. Both M_H and M_L are turned off.,it is also the dead time, the current flows through the body diode D_L (Fig.3(d)). When M_H is turned off and M_L is turned on, the current commutates from the body diode D_L to M_L (Fig.3(e)). The current direction is negative as shown in Fig.4(a)-(e).

According to the above analysis, at the end of the dead time, the reverse recovery phenomenon of the body diode occurs that the current is transferred from the body diode to another MOSFET. When the current is transferred from the body diode to the third quadrant of its own MOSFET, there is no switching loss, because this process is zero voltage switching (ZVS). The commutation situation of the SiC half-bridge is determined by the gate drive signal logic and the current direction.

3. INVERTER POWER LOSSES

Fig.5 shows a SiC half-bridge circuit including parasitic capacitance and parasitic inductance. The gate-source capacitance is considered to be a constant value under different drain-source voltages. The gate-drain capacitance and the drain-source capacitance can be expressed as[5]

$$C\left(v_{ds}\right)=\frac{C_{0v}}{\left(1+\frac{v_{ds}}{\varphi}\right)^{\gamma}}+C_{hv} \tag{1}$$

Where, C_{0v} and C_{hv} are the capacitance parameters corresponding to low voltage and high voltage

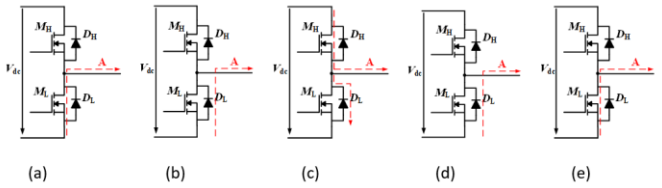


Fig.3 Positive current

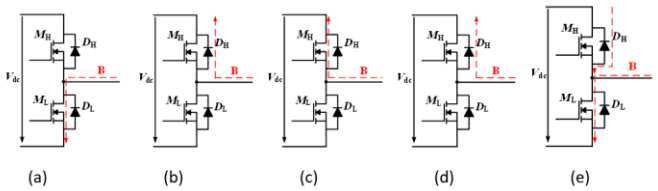


Fig.4 Negative current

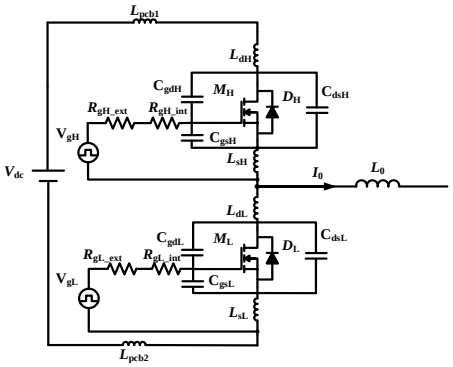


Fig.5 SiC half-bridge circuit considering parasitic parameters

respectively. φ and γ are fitting coefficients according to data sheet.

The transfer characteristics of SiC MOSFET can be expressed as

$$\begin{cases} i_{ch}=0, & v_{gs}<V_{th} \\ i_{ch}=k_{fs}\left(v_{gs}-V_{th}\right)^2, & v_{gs}\geq V_{th} \end{cases} \tag{2}$$

For simplicity, i_{ch} can be linearized as $i_{ch}=g_{fs}\left(v_{gs}-V_{th}\right)$.Generally, g_{fs} is assumed to be a constant value[6],however,transconductance is a function of channel current, expressed as:

$$g_{fs}=f\left(i_{ch}\right) \tag{3}$$

In the following, only the case for positive current is analyzed and the negative current case can be analyzed in the same way. A switching period can be divided into three parts: process I, process II and process III. Here, it is assumed that M_H and M_L have the same parasitic.

$$\begin{cases} C_{issH}=C_{issL}=C_{iss} \\ C_{rssH}=C_{rssL}=C_{rss} \\ C_{ossH}=C_{ossL}=C_{oss} \end{cases} \tag{4}$$

3.1 Loss of the process I

The process I concerns the current commutates from the third quadrant channel of M_L to the body diode D_L.

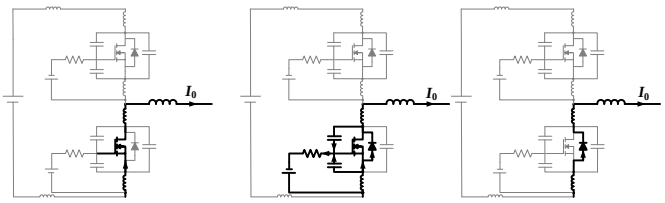


Fig. 6 Current flow paths during process I

3.1.1 stage 1

As shown in Fig. 6(a), before M_L is turned off, the current flows through the third quadrant channel of M_L.The conduction loss expression is following.

$$P_a = I_0^{\,2} \times R_{sd(on)} \tag{5}$$

Where $R_{sd(on)}$ is the third quadrant on-resistance of the SiC MOSFET.

3.1.2 stage 2

This stage is ZVS and the current flows through M_L and the body diode D_L at the same time in Fig. 6(b). Through a first-order model of the gate circuit, this falling time can be given as

$$t_b = R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs\_max} - V_{gs\_min}}{V_{th} - V_{gs\_min}}\right) \tag{6}$$

3.1.3 stage 3

As shown in Fig. 6(c),M_L is completely turned off, all current flows through D_L. The conduction loss of the body diode can be expressed as

$$P_c = V_d \cdot I_0 \cdot (T_d - t_b) \cdot f_{sw} \tag{7}$$

Where V_d is the voltage drop of the body diode; T_d is dead time; f_{sw} is switching frequency.

3.2 Loss of the process II

The current commutates from high side switch M_H to low side switch M_L. The turn-on and turn-off process is analyzed in detail below.Fig.7 is the current flow paths in various stage during process II.Fig.8 is switching transition waveforms.

3.2.1 Turn-on loss

As shown in Fig. 7(a)-(e) and Fig.8(a) , the turn-on process is divided into five periods from t_0 to t_5.

Period 1($t_0 < t < t_1$):This is turn-on delay time, the power loss of this period is still the conduction loss of the body diode.The duration of this period can be obtained by

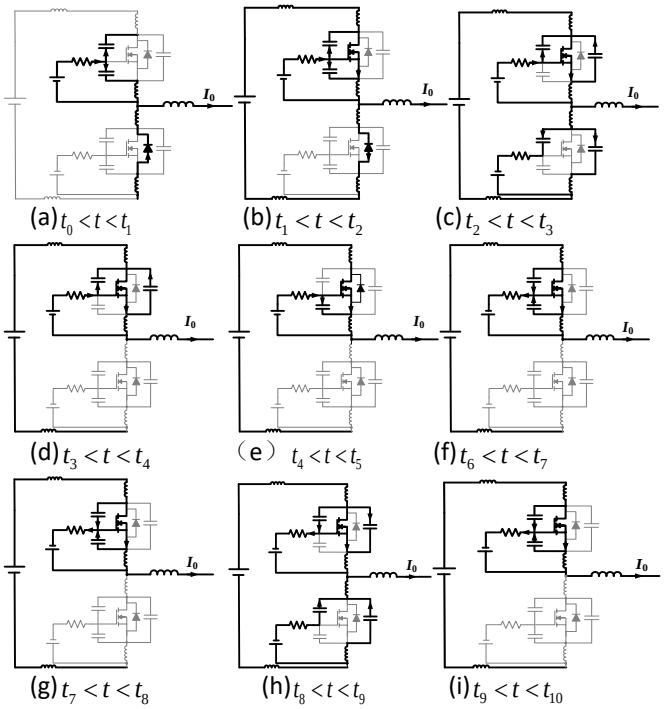


Fig.7 Current flow paths during process II

$$t_1 - t_0 = R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs\_max} - V_{gs\_min}}{V_{gs\_max} - V_{th}}\right) \tag{8}$$

Therefore, combining Eqs.(7) and (8),the loss is rewritten as

$$P_1 = V_d \cdot I_0 \cdot (t_1 - t_0) \cdot f_{sw} \tag{9}$$

Period 2($t_1 < t < t_2$):At t_1,SiC MOSFET starts to conduct. Body diode reverse recovery current increases drain current. The MOSFET works in the saturation area and can be modeled as a voltage-controlled current source.

$$i_{chH}(t) = g_{fs}\left[v_{gsH}(t) - V_{th}\right] \tag{10}$$

At t_2, the gate voltage increases to the miller voltage, which can be expressed as

$$V_{miller} = I_0 / g_{fs} + V_{th} \tag{11}$$

The average gate drive current is expressed as

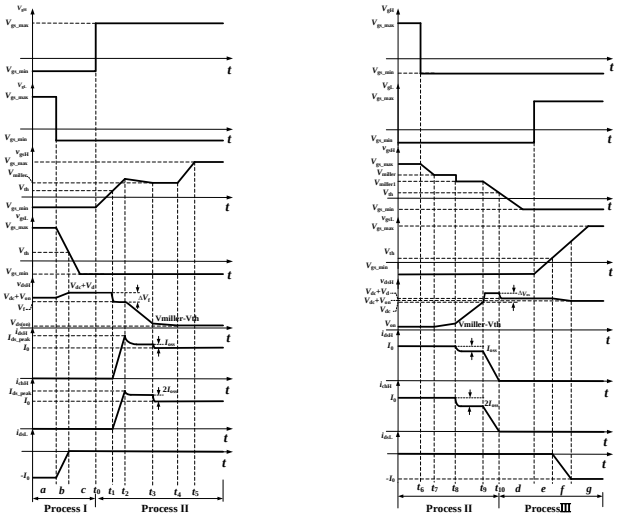
$$i_{g1} = \frac{V_{gs\_max} - \left(V_{miller} + V_{th}\right)/2 - L_{sH}\left(di/dt\right)}{R_g} \tag{12}$$

At t_2,the drain-source voltage of MH is expressed as

$$V_f = V_{dc} + V_d - L_{loop}\frac{di_d}{dt} \tag{13}$$

where L_{loop} is Loop lumped parasitic inductance $L_{loop} = L_{pcb1} + L_{pcb2} + L_{dH} + L_{sH}$.

Hence, according to Eqs.(10)-(13), this period can be calculated.



(a) (b)

Fig.8 switching transition waveforms

$$t_2 - t_1 = \frac{\left[\left(C_{gs} + C_{gd}\right)R_g + L_{sH} g_{fs}\right] I_{d\_peak}}{\left(V_{gs\_max} - V_{th}/2 - V_{miller}/2\right) g_{fs}} \tag{14}$$

The total energy loss during this period is

$$E_2 = \int_{t_1}^{t_2} v_{dsH}(t) i_{chH}(t)\,dt = \frac{1}{2}\left(I_0 + I_{rrm}\right)^2 \left[\left(V_{dc} + V_d\right)\frac{\left[\left(C_{gs} + C_{gd}\right)R_g + L_{sH} g_{fs}\right]}{\left[V_{gs\_max} - V_{th}/2 - V_{miller}/2\right] g_{fs}} - L_{loop}\right] \tag{15}$$

Period 3($t_2 < t < t_3$):The drain-source voltage starts to drop rapidly in the saturation region.As shown in Fig.9(a),

The discharge current of the output capacitor of M_H and the charg current of the output capacitor of M_L. can not be ignored,which can be expressed as

$$\begin{aligned} i_{dH} &= I_0 + I_{oss,M_L} \\ i_{chH} &= i_{dH} + I_{oss,M_H} \end{aligned} \tag{16}$$

The average gate drive current is expressed as

$$i_{g2} = \frac{V_{gs\_max} - v_{gsH}}{R_g} = \frac{V_{gs\_max} - V_{th} - \frac{1}{g_{fs}}\left[I_0 + 2\left(C_{gd} + C_{ds}\right)\frac{V_{dc} + V_d - V_{miller} + V_{th}}{\left(t_3 - t_2\right)}\right]}{R_g} \tag{17}$$

According to Eqs.(16)-(17), this period can be calculated.

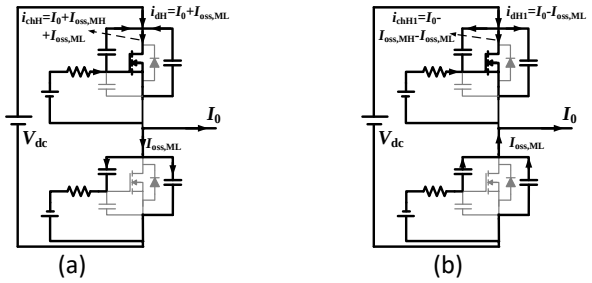
$$t_3 - t_2 = \frac{\left(V_f + V_{th} - V_{miller}\right) R_g C_{gd} + \left[2\left(C_{gd} + C_{ds}\right)\left(V_{dc} + V_d - V_{miller} + V_{th}\right)\right]/g_{fs}}{V_{gs\_max} - V_{miller}} \tag{18}$$

In addition, body diode reverse recovery loss can be expressed as[3]

$$\begin{cases} Q_{rr} = Q_{rr\_1} + Q_{rr\_2} \\ Q_{rr\_1} = T_a I_{rrm}/2 \\ di_d/dt = I_{rrm}/T_a \\ E_{rr\_2} = \left(V_f + V_{miller} - V_{th}\right) Q_{rr\_2}/2 \end{cases} \tag{19}$$

This part of energy loss can be calculated by

$$E_3 = \int_{t_2}^{t_3} v_{dsH}(t) i_{chH}(t)\,dt = \frac{\left(I_0 + 2I_{oss}\right)\left(V_f - V_{miller} + V_{th}\right)\left[\left(V_f - V_{miller} + V_{th}\right) R_g C_{gd} g_{fs} + 2\left(C_{gd} + C_{ds}\right)\left(V_{dc} + V_d - V_{miller} + V_{th}\right)\right]}{2 g_{fs}\left(V_{gs\_max} - V_{miller}\right)} + \frac{\left(V_f + V_{miller} - V_{th}\right) Q_{rr\_2}}{2} \tag{20}$$



(a) (b)

Fig.9 Parasitic capacitance charge and discharge current path
(a) Turn-on of M_H (b) Turn-off of M_H

Period 4($t_3 < t < t_4$):The MOSFET works in resistance area.The drain-source voltage continues to decrease until it reaches the turn-on voltage drop of the SiC MOSFET. The average gate drive current is expressed as

$$i_{g3} = \frac{V_{gs\_max} - V_{miller}}{R_g} \tag{21}$$

The total energy loss during this period is

$$E_4 = \int_{t_3}^{t_4} v_{dsH}(t) i_{chH}(t)dt = \frac{I_0\left(V_{miller} - V_{th} - V_{ds(on)}\right)^2 C_{gd} R_g}{2\left(V_{gs\_max} - V_{miller}\right)} \tag{22}$$

where

$$t_4 - t_3 = \frac{\left(V_{miller} - V_{th} - V_{ds(on)}\right) C_{gd} R_g}{V_{gs\_max} - V_{miller}} \tag{23}$$

Period 5($t_4 < t < t_5$):At t_4, SiC MOSFET has turned on completely. The drain current remains the same load current despite the increase of v_{gsH} .During this period, there is no switching loss. The conduction loss can be expressed as

$$P_5 = I_0^{\,2} \times R_{ds(on)} \tag{24}$$

where $R_{ds(on)}$ is on-resistance of the SiC MOSFET.

3.2.2Turn-off loss

As shown in Fig. 7(f)-(i) and Fig.8(b), the turn-off process is divided into four periods from t_6 to t_{10}.

Period 6($t_6 < t < t_7$ **)**:This is turn-on delay time, SiC MOSFET is still completely turned on and it is handling the load current. During this period, there is no switching loss occurring,the power loss of this period is still the conduction loss. This period can be expressed as

$$t_7 - t_6 = R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs\_max} - V_{gs\_min}}{V_{miller} - V_{gs\_min}}\right) \tag{25}$$

Period 7($t_7 < t < t_8$ **)**:SiC MOSFET still works in the resistance region.At t_8, the drain-source voltage increases to $V_{miller} - V_{th}$,at the same time, MOSFET works into the saturation region. Drain current stays the maximum load current. The average gate drive current is expressed as

$$i_{g4} = \frac{V_{miller} - V_{gs\_min}}{R_g} \tag{26}$$

The loss during this turn-off can be calculated by

$$E_7=\int_{t_7}^{t_8} v_{\mathrm{dsH}}(t)\,i_{\mathrm{chH}}(t)dt=\frac{I_0\left(V_{\mathrm{miller}}-V_{\mathrm{th}}-V_{\mathrm{ds(on)}}\right)^2 C_{\mathrm{gd}}R_{\mathrm{g}}}{2\left(V_{\mathrm{miller}}-V_{\mathrm{gs\_min}}\right)} \tag{27}$$

where

$$t_8-t_7=\frac{\left(V_{\mathrm{miller}}-V_{\mathrm{th}}-V_{\mathrm{ds(on)}}\right)C_{\mathrm{gd}}R_{\mathrm{g}}}{V_{\mathrm{miller}}-V_{\mathrm{gs\_min}}} \tag{28}$$

Period 8($t_8<t<t_9$):The drain-source voltage increases to DC bus voltage at the end of this period.As shown in Fig.9(b), parasitic capacitance charge and discharge current should be taken into account, which can be expressed as

$$\begin{aligned} i_{\mathrm{dH1}}&=I_0-I_{\mathrm{oss,M_L}}\\ i_{\mathrm{chH1}}&=i_{\mathrm{dH1}}-I_{\mathrm{oss,M_H}} \end{aligned} \tag{29}$$

The average gate drive current is expressed as

$$i_{\mathrm{g5}}=\frac{v_{\mathrm{gsH}}-V_{\mathrm{gs\_min}}}{R_{\mathrm{g}}} \tag{30}$$

Therefore, combining Eqs.(28) and (29), this period is rewritten as

$$t_9-t_8=\frac{C_{\mathrm{gd}}R_{\mathrm{g}}\left(V_{\mathrm{dc}}-V_{\mathrm{miller}}+V_{\mathrm{th}}\right)+\left[2\left(C_{\mathrm{gd}}+C_{\mathrm{ds}}\right)\left(V_{\mathrm{dc}}-V_{\mathrm{miller}}+V_{\mathrm{th}}\right)/g_{\mathrm{fs}}\right]}{V_{\mathrm{miller}}-V_{\mathrm{gs\_min}}} \tag{31}$$

The total energy loss during this period is

$$E_8=\int_{t_8}^{t_9} v_{\mathrm{dsH}}(t)\,i_{\mathrm{chH}}(t)dt=\frac{\left(I_0-2I_{\mathrm{oss}}\right)\left\{C_{\mathrm{gd}}R_{\mathrm{g}}\left(V_{\mathrm{dc}}-V_{\mathrm{miller}}+V_{\mathrm{th}}\right)^2+\left[2\left(C_{\mathrm{gd}}+C_{\mathrm{ds}}\right)\left(V_{\mathrm{dc}}-V_{\mathrm{miller}}+V_{\mathrm{th}}\right)^2/g_{\mathrm{fs}}\right]\right\}}{2\left(V_{\mathrm{miller}}-V_{\mathrm{gs\_min}}\right)} \tag{32}$$

Period 9($t_9<t<t_{10}$):At t_{10}, the drain-source current is reduced to 0. Due to parasitic inductance, the drain-source voltage can be expressed as

$$v_{\mathrm{dsH}}=V_{\mathrm{dc}}+\Delta V_{\mathrm{os}}=V_{\mathrm{dc}}+L_{\mathrm{loop}}\frac{di_{\mathrm{dH}}}{dt}=V_{\mathrm{dc}}+L_{\mathrm{loop}}\frac{I_0-I_{\mathrm{oss}}}{\left(t_{10}-t_9\right)} \tag{33}$$

The average gate drive current is expressed as

$$i_{\mathrm{g6}}=\frac{1/2\left(V_{\mathrm{miller1}}+V_{\mathrm{th}}\right)-V_{\mathrm{gs\_min}}-L_{\mathrm{sH}}\,di_{\mathrm{d}}/dt}{R_g} \tag{34}$$

The loss during this turn-off can be calculated by

$$E_9=\int_{t_9}^{t_{10}} v_{\mathrm{dsH}}(t)\,i_{\mathrm{chH}}(t)dt=\frac{\left(I_0-2I_{\mathrm{oss}}\right)\left\{2R_{\mathrm{g}}V_{\mathrm{dc}}\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right)\left(V_{\mathrm{miller1}}-V_{\mathrm{th}}\right)+\left(I_0-I_{\mathrm{oss}}\right)\left[2V_{\mathrm{dc}}L_{\mathrm{sH}}+L_{\mathrm{loop}}\left(V_{\mathrm{miller1}}+V_{\mathrm{th}}-2V_{\mathrm{gs\_min}}\right)\right]\right\}}{2\left(V_{\mathrm{miller1}}+V_{\mathrm{th}}\right)-4V_{\mathrm{gs\_min}}} \tag{35}$$

3.3Loss of the process III

The process I concerns the current commutates from the body diode D_L to the third quadrant channel of M_L. It is a reverse of process I, this process is no longer analyzed.

4. SIMULATION RESULTS

The SiC half-bridge circuits were simulated in LTspice using the manufacturers' Spice models of the SiC MOSFET(C2M0025120D).

Table I Nonlinear capacitance fitting coefficient

Capacitance	Parameter	Value	Parameter	Value
C_{oss}	φ	11.4	C_{0v}	3180pF
	γ	1.27	C_{hv}	220pF
C_{rss}	φ	10.8	C_{0v}	985pF
	γ	1.65	C_{hv}	15pF

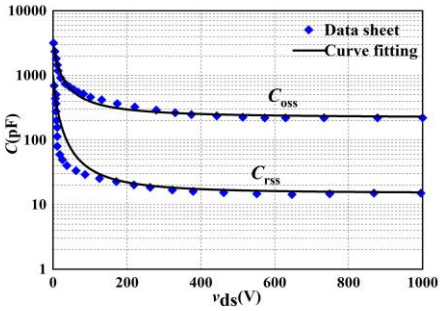


Fig.10 Nonlinear capacitance fitting curve

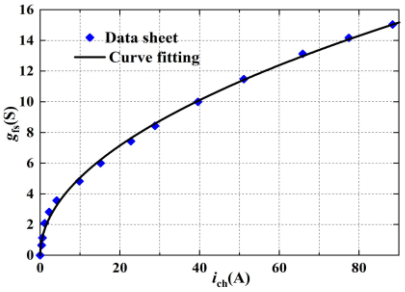


Fig.11 Relationship between transconductance and current

4.1 Parasitic parameter extraction

The fitting coefficients of SiC MOSFET nonlinear capacitance are shown in Table I. As shown in Fig.10, the fitting results are in good agreement with the data extracted in the data sheet.

Figure 11 shows the relationship between transconductance and channel current, which can be expressed as:

$$g_{\mathrm{fs}}=k_1 i_{\mathrm{ch}}^{\,k_2} \tag{36}$$

Where k_1=1.6 , k_2=0.5 .

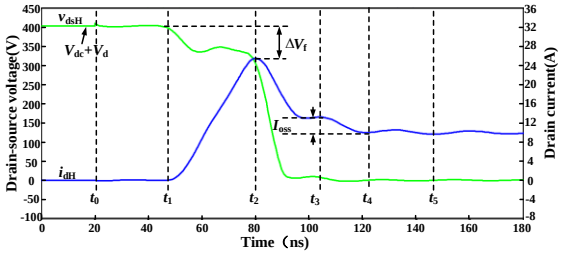
Simulation and analysis model parameters are shown in Table II.

4.2 Simulation results

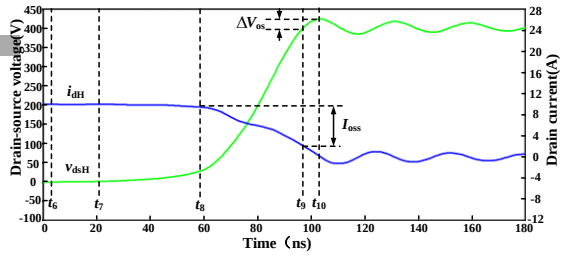
LTspice simulation transients for SiC MOSFET at 400 V 10 A are shown in Fig.12. The simulation results are consistent with the aforementioned analysis process. To verify the correctness of the analysis model，switching losses at different operating points are calculated. Fig. 13 (a) and (b) are the switching losses under different resistances and currents, respectively. As shown in Fig.13, the simulation loss and the calculated value of the analysis model under different working conditions have

Table II Parameters Values

Type	Parameter	Value	Parameter	Value
Power circuit	V_{dc}	400V	I_0	10A
	L_{pcb1}	27nH	L_{pcb2}	22nH
Drive circuit	V_{gs_max}	20V	V_{gs_min}	-5V
	R_{g_ext}	20Ω	R_{g_int}	1.1Ω
SiC MOSFET	R_{ds} / R_{sd}	25mΩ	V_{th}	2.6V
	L_d	6nH	L_s	9nH
	C_{gs}	2773pF		
Body diode	Q_{rr}	409nC	V_d	3.3V
	I_{rrm}	13.5A		



(a)



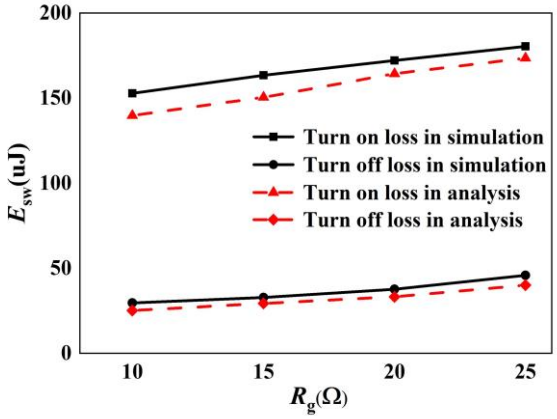
(b)

Fig.12 switching transition waveforms in simulation
(a) Turn-on (b)Turn-off

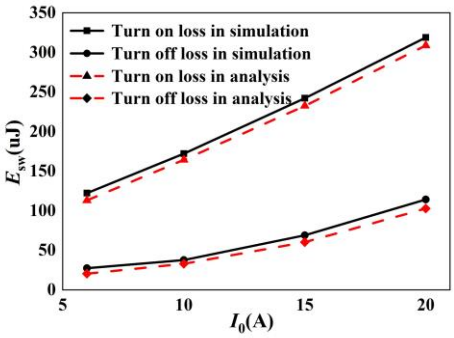
good consistency, and the analysis model can be used to estimate the switching loss.

5.CONCLUSIONS

This paper firstly analyzes the commutation mechanism of SiC MOSFET half-bridge in EV traction system. SiC MOSFETs switching process are investigated in detail and switching losses are modeled,which includes parasitic inductance, parasitic capacitance nonlinearity, transconductance nonlinearity, body diode reverse recovery, and parasitic capacitance charging and discharging comprehensively. Finally, the simulation results verify the correctness of the analysis model.



(a)



(b)

Fig.13 Comparison of simulation and calculation losses under different conditions
(a) Different resistance (b) Different current

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